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in their Hardware Description Language (HDL) which promotes the repetition of evolved use. 1 Introduction Research into the use of **evolutionary algorithms** (EAs) for the optimisation and Research into the use of **evolutionary algorithms** (EAs) for the optimisation and solution of ftp.cogs.susx.ac.uk/pub/reports/csrp/csrp479.ps.Z

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in a hardware description language such as VHDL [9] This behavioral description forms the basis presented in this paper. An approach based upon **evolutionary** programming for an area efficient design of optimization problems. We introduce a genetic **algorithm** with a new chromosomal representation of data www.informatik.uni-dortmund.de/publications/papers/1997-iss.ps.gz

[Synthesis of Communicating Controllers for Concurrent.. - Niemann Marwedel \(1998\)](#) [\(Correct\)](#)

The way of specifying systems (based on a subset of VHDL) and the partitioning **algorithms** have been problem, e.g. dynamic programming, **evolutionary** strategies, mixed integer linear programming has been explored intensively, using different **algorithms** to solve this complex optimization problem, www.informatik.uni-dortmund.de/publications/papers/1998-date-niemann.ps.gz

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[3] B. L. Hutchings and M. J. Wirthlin. Implementation approaches for
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Promises and Challenges of Evolvable Hardware - Yao (1996) (Correct) (15 citations)

approach is the evolution of a binary adder using HDL (Hard ware Description Language) programs [11]
 environment. At present, almost all EHW uses an evolutionary algorithm (EA) as their main adaptive
 hardware. According to different EAs, e.g. genetic algorithms (GAs) genetic programming (GP)
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and parsing programs, PERL for text manipulation, VHDL for hardware description, TeX and LaTeX for
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 www.cs.yale.edu/HTML/YALE/CS/HyPlans/hudak-dir/icsr98.ps

HGA: A Hardware-Based Genetic Algorithm - Scott (1994) (Correct) (14 citations)

Corporation, Wilsonville, Oregon. AutoLogic VHDL Synthesis Guide, 1993. 18] Mentor Graphics
 design entry methods like this are only feasible if HDL synthesis tools are available. If one wants to go
 102 [19] Heinz Muhlenbein. Evolutionary algorithms: Theory and applications.
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circuits using a hardware description language (HDL) In DARWIN (Kruiskamp and Leenaerts 1995) opamp
 mutation to create offspring. This automated evolutionary process produces both the topology of the
 And Sizing Of Analog Electrical Circuits Using Genetic Programming John R. Koza, Forrest H Bennett Iii,
 www.genetic-programming.com/AID96.ps

A Hardware Genetic Algorithm for the Traveling Salesman Problem.. - Graham (1995) (Correct) (9 citations)

[3] P. Graham and B. Nelson, A hardware genetic algorithm for the traveling salesman problem on
 England, pp. 352-361, August 1995. A Hardware Genetic Algorithm for the Traveling Salesman Problem on
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A Hardware Engine for Genetic Algorithms - Scott, Seth, Samal (1997) (Correct) (7 citations)

as a proof of concept system. It was designed using VHDL to allow for easy scalability. It is designed to
 spC compiler [19] Flamel [20] Cyber [21] or an HDL synthesizer such as IBM's HIS system [22] or
 using a genetic algorithm, in Progress in Evolutionary Computation, X. Yao, Ed. Berlin, 1995, pp.
 ftp.cse.unl.edu/pub/TechReps/UNL-CSE-97-001.ps.gz

A Synthesizable VHDL Coding of a Genetic Algorithm - Scott, Seth, Samal (1997) (Correct) (7 citations)

A Synthesizable VHDL Coding of a Genetic Algorithm Technical Report
 inputs and outputs. For example, in the file fitness.hdl, ain is an input (due to the keyword IN) is of
 algorithm. In X. Yao, editor, Progress in Evolutionary Computation, pages 109-126, Berlin, 1995.
 www.cse.unl.edu/~sscott/research/papers/UNL-CSE-97-009.ps.gz

Toward Evolution of Electronic Animals Using Genetic Programming - John Koza (Correct) (7 citations)

circuits using a hardware description language (HDL) The design of analog circuits and mixed
 The user supplied fitness measure drives the evolutionary process. In general, the fitness measure may
 Toward Evolution of Electronic Animals Using Genetic Programming John R. Koza Computer Science Dept.
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 circuits using a hardware description language (HDL)The design of analog circuits and mixed
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 Problems for which a Computer Program Evolved by **Genetic** Programming is Competitive with Human
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Testability analysis and ATPG on behavioral RT-level VHDL - Corno, Prinetto, Reorda (1997) (Correct) (5 citations)
 Testability Analysis And Atpg On Behavioral Rt-Level Vhdl Fulvio Corno, Paolo Prinetto, Matteo Sonza
 Reorda
 evaluation, etc. more and more resort to behavioral HDL descriptions. The main reason why testability
 cycle. A prototype tool called RAGE (RT-level **genetic** Algorithm for test pattern GEneration) is used
www.cad.polito.it/pap/db/itc97.ps.gz

An Implementation of GEM -- supporting a semantic data.. - Shalom Tsurli Carlo (1984) (Correct) (4 citations)
 [26] Shalom Tsur and Carlo Zaniolo. An implementation of gem -
www.cs.ucla.edu/~zaniolo/papers/sigmod94.pdf

A VHDL Error Simulator for Functional Test Generation - Alessandro Fin Franco (2000) (Correct) (3 citations)
 A VHDL Error Simulator for Functional Test Generation
 by means of a hardware description language (HDL)such as VHDL [7] or Verilog [8]Such techniques
www.sigda.org/Archives/ProceedingArchives/Date/Date2000/papers/2000/date00/htmlfiles/sun_sgi/.../pdffiles/05

Exploiting Behavioral Information in Gate-level ATPG - Silvia Chiusano Fulvio (1999) (Correct) (3 citations)
 by the relative simplicity of behavioral-level VHDL primitives with respect to the one available in
 of a design, and because of the similarity between HDL description and software program, we derived
 Synthesis, High Level Test, Software Testing, **Genetic** Algorithms, Simulated Annealing Abstract This
www.cad.polito.it/pap/db/jetta98.ps.gz

Hardware Software Partitioning with Integrated Hardware.. - Vinoo Srinivasan Shankar (1998) (Correct) (3 citations)
 and a software code segment. In our case, we use vhdl and c to rep resent the hardware and software
 presents a **Genetic** Algorithm (ga) 15] based **evolutionary** approach to hardwaresoftware partitioning and
 hardware design space exploration. We propose a **genetic** algorithm which performs hardware software
www.ece.uc.edu/~ddel/publications/srinivasan-date-98.ps

Armstrong III: A Loosely-Coupled Parallel Processor .. - Wazlowski, Smith.. (1996) (Correct) (3 citations)
 x 16 crossbar switch. Applications are developed in VHDL. Many applications have been implemented on the
 been implemented on the Splash 2 system including **genetic** database searches and realtime
 imageprocessing
ftp.lems.brown.edu/pub/arm/papers/tech_rep94_2.ps.gz

Evolvable Hardware with Genetic Learning - Tetsuya Higuchi (1994) (Correct) (3 citations)
 the gatelevel hardware evolution [2,6] and the HDL (Hard ware Description Language) level hardware
 Evolvable Hardware with **Genetic** Learning \Lambda Tetsuya Higuchi
 (EHW)The adaptation process is a combination of **genetic** learning with reinforcement learn ing. A first
jisp.cs.nyu.edu/RWC/rwcp/papers/1994/A-21_067.ps.gz

Explorer: An Interactive Floorplanner for Design Space.. - Esbensen, Kuh (1996) (Correct) (2 citations)
 approach described in [3]EURO-DAC '96 with EURO-VHDL '96 0-89791-848-7/96 \$4.00 1996 IEEE 2 Problem
 Abstract An interactive floorplanner based on the **genetic** algorithm is presented. Layout area, aspect
 the problem [7]3 Explorer is based on the **genetic** algorithm (GA)since it is particularly well
herkules.informatik.tu-chemnitz.de/proceedings/eurodac-96/papers/1996/eurdac96/htmlfiles/sun_sgi/.../pdffiles/d

High-Level Observability for Effective High-Level ATPG - Fulvio Corno Matteo (2000) (Correct) (2 citations)

knowledge gathered during a static analysis of the **VHDL** source and the dynamic information coming from
Some approaches rely on a direct examination of the **HDL** description [CCPr98] or exploit the knowledge of
system called ARTIST. Such system is based on a **Genetic** Algorithm that exploits the knowledge gathered
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